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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Steve Nishimoto	§	Group Art Unit:	2189
Serial No.:	09/541,780	§	Examiner:	Christopher E. Lee
Filed:	April 3, 2000	§		
For:	Circuit and Technique to Stall the Communication of Data Over a Double Pumped Bus	§	Atty. Dkt. No.:	ITL.0349US (P8539)

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APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated September 25, 2002, finally rejecting claims 1-23.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010722/0841.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit: February 18, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Board of Patent Appeals & Interferences, Commissioner for Patents, Washington, DC 20231.

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III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-23. An Amendment is currently being submitted with this appeal brief to correct a typographical error in claim 10. Because the Amendment is directed to correcting a typographical error and further narrows down the issues on appeal, it is assumed for purposes of this appeal that the Amendment will be entered. Claims 1-23 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

An Amendment is being filed concurrently herewith to correct a typographical error in claim 10, as noted above in the STATUS OF THE CLAIMS section. It is assumed for purposes of this appeal that the Amendment will be entered.

V. SUMMARY OF THE INVENTION

Referring to Fig. 9, an embodiment 100 of a double pumped bus cell in accordance with the invention may be set up to communicate either one or two sets of data. More specifically, in some embodiments of the invention, an EN signal that is received by the cell 100 may be asserted (driven high, for example) to enable the cell 100 to latch, store and retransmit bits of data from two different data sets in a time multiplexed fashion. In this manner, a data line 107 communicates a signal (called DATAIN) that indicates bits of data from a first data set and a second data set. The bits

of the first data set are interleaved, or alternate, in time with the bits of the second data set. Specification, p. 4.

In some embodiments of the invention, when the EN signal is asserted, a bit latch 102 of the cell 100 latches bits one at a time (from the data input line 107) from a first data set in response to the negative edges of a clock signal (called CLK), and another bit latch 104 of the cell 100 latches bits one at a time (also from the data input line 107) from a second data set in response to the positive edges of the CLK signal. The bit latch 102 provides an indication of its latched bit during the logic zero state of the CLK signal, and the bit latch 104 provides an indication of its latched bit during the logic one state of the CLK signal. The select terminal of a multiplexer 106 of the cell 100 receives the CLK signal, selects the output terminal of the bit latch 102 during the logic zero state of the CLK signal and selects the output terminal of the bit latch 104 during the logic one state of the CLK signal. The output terminal of the multiplexer 106 is coupled (via a signal buffer 110) to an output terminal 170 of the cell 100. Thus, due to this arrangement, the cell 100 furnishes the bits of the first and second data sets in a time multiplexed fashion to the output terminal 170 that may be coupled to a double pumped bus wire, for example. Specification, p. 4.

It is noted that, at least in some embodiments of the invention, the cell 100 receives bits from the first data set during the logic one states of the CLK signal, latches these bits in response to the negative edges of the CLK signal and furnishes these bits to the output terminal 170 during the logic zero states of the CLK signal. The cell 100

receives bits from the second data set during the logic zero states of the CLK signal, latches these bits in response to the positive edges of the CLK signal and furnishes these bits to the output terminal 170 during the logic one states of the CLK signal. Thus, the cell 100 reverses the phases between the incoming and outgoing data streams. Specification, pp. 4-5.

It is possible that in a particular scenario, it may not be desirable to communicate both sets of data through the cell 100. For example, in some embodiments, the EN signal may be de-asserted (driven low, for example) to disable the bit latch 104 from latching new bits of data (from the second data set) from the data input line 107. Thus, by disabling the bit latch's ability to receive bit updates, the flow of the second set of data may be effectively halted through the cell 100. Specification, p. 5.

Thus, the double pumped cell 100 may be used in at least two ways. In a chain of double pumped cells, the EN signal may be asserted in each of the cells to enable the communication of both sets of data through the chain. As described above, in some embodiments of the invention, the operation of the bit latch 102 is not affected by the EN signal, as the bit latch 102 responds to the CLK signal, regardless of the state of the EN signal. When the EN signal is asserted for a particular cell 100, both sets of data propagate though the bit latches 102 and 104. Thus, as an example, a particular bit propagates through the bit latch 102 of one cell in the chain, propagates through the bit latch 104 of the next cell in the chain, propagates through the bit latch 102 of the next cell in the chain, etc. The double pumped cell 100 may also be used in the chain to filter out

the communication of one of the sets of data through the chain. For this arrangement, the EN signal is deasserted in every other cell to alternate which bit latch 102, 104 is disabled, as bits of a particular data set alternate between the bit latches 102 and 104 as the data propagates through the chain. Specification, p. 5.

To accomplish the above-described features, in some embodiments of the invention, the cell 100 may include logic, such as an AND gate 112, that receives the CLK and EN signals. The output terminal of the AND gate 112 is coupled to the inverting clock input terminal of the bit latch 104, and the clock input terminal of the bit latch 106 receives the CLK signal. Because the bit latches 102 and 104, in some embodiments of the invention, invert the logic levels of the stored bits, the cell 100 may include an inverter 108 that is coupled between the data input line 107 and the input terminals of the bit latches 102 and 104. When the EN signal is de-asserted, the output terminal of the AND gate 112 is de-asserted, regardless of the logic level of the CLK signal, and thus, the bit latch 104 does not store any new data as long as the EN signal remains de-asserted. However, when the EN signal is asserted, the CLK signal controls the signal at the output terminal of the AND gate 112 and thus, controls the reception of data into the bit latch 104. Specification, pp. 5-6.

Fig. 10 depicts a more detailed schematic diagram of the cell 100 in accordance with some embodiments of the invention. As shown, the bit latch 102 may include a circuit 140 that is effectively a complementary metal oxide semiconductor (CMOS) inverter that is enabled when the CLK signal (that alternates between logic one and logic

zero states) is in a logic one state to latch the bit that is indicated by the DATAIN signal. To accomplish this, the circuit 140 includes an n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) 148 that has its source terminal coupled to ground and its drain terminal coupled to the source terminal of another NMOSFET 146. The drain terminal of the NMOSFET 146 is coupled to the drain terminal of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) 144. The source terminal of the PMOSFET 144 is coupled to the drain terminal of another PMOSFET 142, and the drain terminal of the PMOSFET 142 is coupled to a positive voltage supply level (called V_{DD}). The gate terminals of the PMOSFET 144 and the NMOSFET 146 respond to the logical state of the CLK signal to control when the circuit 140 is enabled. In this manner, the gate terminal of the PMOSFET 144 is coupled to a clock input terminal 131 (that furnishes the CLK signal) via a chain 124 of three serially coupled inverters 240 that invert the CLK signal to receive an inverted version of the CLK signal. The gate terminal of the NMOSFET 146 is coupled to a chain 123 of serially coupled inverters 120 to the clock line 131 to receive an indication of the CLK signal. The gate terminals of the PMOSFET 144 and the NMOSFET 148 are coupled to the data input line 107. Specification, p. 6.

For purposes of storing the bit inside the bit latch 102, the buffer 102 includes a latch circuit that is formed by two inverters 160 and 162 that are coupled together in a back-to-back arrangement. The input terminal of the inverter 160 and the output terminal of the inverter 162 are coupled together to the drain terminal of the NMOSFET 146. An

inverter 164 is coupled between the drain terminal of the NMOSFET 146 and the multiplexer 106. Thus due to this arrangement, when the circuit 140 is enabled during the logic one state of the CLK signal, the CMOS inverter (formed by the transistors 142, 144, 146 and 148) drives the inverters 160 and 162 to update the state of the stored bit, and when the CLK signal transitions from the logic one to the logic zero state on a negative edge, the CMOS inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162. Specification, pp. 6-7.

Similar to the bit latch 102, the bit latch 104 includes the circuit 140 and the bit latch that is formed from inverters 160 and 162. However, unlike the bit latch 102, the gate terminals of the circuit 140 of the bit latch 140 are connected differently. In this manner, the gate terminal of the PMOSFET 144 is coupled to the output terminal of a NAND gate 124, and the gate terminal of the NMOSFET 146 is coupled to the output terminal of an inverter 136 that has its input terminal coupled to the output terminal of the NAND gate 124. One input terminal of the NAND gate 124 is coupled between the inverter 120 to receive an inverted indication of the CLK signal, and the other input terminal of the NAND gate 124 is coupled to an enable input line 113 to receive the EN signal. Thus, when the EN signal is asserted, the circuit 140 of the bit latch 104 is enabled during the logic zero state of the CLK signal to update the bit that is stored by the inverters 166 and 168 of the circuit 140. During the logic one state of the CLK signal and when the EN signal is de-asserted, the circuit 140 is disabled. Thus, when the CLK signal transitions from the logic zero to the logic one state on a positive edge, the CMOS

inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162 of the bit latch 104. Specification, p. 7.

In some embodiments of the invention, the multiplexer 106 includes two CMOS pass gates 172 and 174. The input terminal of the CMOS pass gate 172 is coupled to the output terminal of the inverter 164 of the bit latch 102, and the output terminal of the CMOS pass gate 172 is coupled to a node 168 that forms the output terminal of the multiplexer 106. The inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the NMOSFET 146 of the bit latch 102, and the non-inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the PMOSFET 144 of the bit latch 102. Thus, due to this arrangement, the output terminal of the bit latch 102 is coupled to the output terminal of the multiplexer 160 when the CLK signal has a logic zero level. The input terminal of the CMOS pass gate 174 is coupled to the output terminal of the inverter 164 of the bit latch 104, and the output terminal of the CMOS pass gate 174 is coupled to the node 168. The inverting control terminal of the pass gate 174 is coupled to the non-inverting control terminal of the pass gate 172, and the non-inverting control terminal of the pass gate 174 is coupled to the inverting control terminal of the pass gate 172. Thus, due to this arrangement, the output terminal of the bit latch 104 is coupled to the output terminal of the multiplexer 160 when the CLK signal has a logic one level. In some embodiments of the invention, the inverter 110 may include a chain of three inverters 109 that are coupled between the node 168 and the output terminal 170. Specification, pp. 7-8.

The cell 100 that is described above receives time-multiplexed bits of data from a single wire. However, in some embodiments of the invention, a cell 200 that is depicted in Fig. 11 may be used in place of the cell 100. The cell 200 has a similar design to the cell 100 except for the following features. Unlike the cell 100, the cell 200 has two data input lines 203 and 205 (instead of one) to receive bits of data from circuits that are associated with two different data sets. In this manner, the inverter 108 (see Fig. 9) of the cell 100 is replaced by two inverters 202 and 207 of the circuit 200. The input terminal of the inverter 202 receives a signal (called DATA1) that is indicative of bits of data from the first data set, and the input terminal of the inverter 207 receives a signal (called DATA2) that is indicative of bits of data from the second data set. The output terminal of the inverter 202 is coupled to the data input line of the bit latch 102, and the output terminal of the inverter 207 is coupled to the data input line of the bit latch 104. Specification, p. 8.

Referring to Fig. 12, in some embodiments of the invention, the cells 100 (the enabled cells 100a and the disabled cells 100b, as described below) and 200 may be used to form a double pumped bus chain 220 for purposes of communicating the bits of data from the first and second data sets across an integrated circuit, for example. In this manner, the cell 200 is the first in the chain 220 to arrange bits from the two different data sets in a time interleaved fashion. The cells 100 may be serially coupled together after the cell 200. As shown, to disable the flow of the bits of the data set that is associated with the DATA2 signal, every other cell 100 is disabled, as depicted in Fig. 12

by the enabled cells 100a and the disabled cells 100b. This alternative disabling of the cells 100 occurs because each cell 100 reverses the phasing of the data flow. For example, each cell 100 receives the bits of a particular data set on positive clock edges and retransmits the bits of that data set on negative clock edges. The arrangement that is depicted in Fig. 12 is used to disable the flow of bits for the data set that is associated with the DATA2 signal. However, alternatively, to disable the bits for the data set that is associated with the DATA1 signal, the enable input terminals 113 of the cells 200 and 100b are asserted, and the enable input terminals 113 of the cells 100a are de-asserted. Specification, pp. 8-9.

Referring to Fig. 13, as an example, the cell 200 (and/or the cell 100) may be used in a semiconductor circuit, such as a processor 252 (a microprocessor, such as a Pentium® microprocessor, as an example), to communicate bits of data between circuits 254, 256, 260 and 262 of the processor 252. In this manner, the cell 200 may communicate data over a wire 258 for two data sets. More specifically, the cell 200 may communicate data for a first data set between the circuit 254 that is located at one end of the wire 258 and the circuit 260 that is located at another end of the wire 268. The cell 200 may also communicate data for a second data set between the circuit 256 that is located at one end of the wire 258 and the circuit 262 that is located at the other end of the wire 268. Specification, p. 9.

Among the other components of the computer system 250, the computer system 250 may include a local bus 270 that is coupled to the processor 252 and is also coupled

to a north bridge, or memory hub 272. As an example, the memory hub 272 may provide interfaces for a Peripheral Component Interface (PCI) bus 284, an Accelerated Graphics Port (AGP) bus 286 and a memory bus 276. The AGP is described in detail in the Accelerated Graphics Port Interface Specification, Revision 1.0, published on July 31, 1996, by Intel Corporation of Santa Clara, California. The PCI Specification is available from The PCI Special Interest Group, Portland, Oregon 97214. The memory bus 276 communicates data between the memory hub 272 and a system memory 274. A display controller 287 may be coupled the AGP bus 286 and drive a display 289. A hub bus 289 may establish communication between the memory hub 272 and a south bridge, or input/output (I/O) hub 290. Specification, p. 9.

The I/O hub 290 may, for example, control operation of a CD-ROM drive 292 and a hard disk drive 294. The I/O hub 290 may also provide an interface to an I/O expansion bus 296. An I/O controller 298 may be coupled to the I/O expansion bus 296. The I/O controller 298 may, for example, receive input data from a mouse 300 and a keyboard 302 and control operation of a floppy disk drive 304. The computer system 250 is one out of many different embodiments, all of which are within the scope of the appended claims. Specification, p. 9.

VI. ISSUES

A. Can claims 1-9 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 1?

B. Can claims 10-14 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 10?

C. Can claims 15-19 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 15?

D. Can claim 16 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 16?

E. Can claims 20-23 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 20?

VII. GROUPING OF THE CLAIMS

Claims 1-9 can be grouped together; claims 10-14 can be grouped together; claims 15 and 17-19 can be grouped together; claims 20-23 can be grouped together; and claim 16 is separately patentable for the reasons set forth below.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-9 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 1?

The apparatus of claim 1 includes a first circuit and a second circuit. The first circuit receives indications of first data that is associated with a first data set and second data that is associated with a second data set. The second circuit is coupled to the first

circuit to cause the first circuit to in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal. The second circuit also causes the first circuit to in a second mode, communicate indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) in view of the combination of U.S. Patent No. 6,049,883 (herein called "Tjandrasuwita") and alleged Applicant's admitted prior art (herein called "AAPA"). Tjandrasuwita generally teaches a clock gating apparatus.

More specifically Tjandrasuwita teaches a latch circuit 502 (Fig. 5) that receives a clock signal from an AND gate 503. The AND gate 503, in turn, receives a clock signal and an enable signal called EN2. *See generally,* Tjandrasuwita, 6:30-60. Tjandrasuwita discloses that the clock signal to the latch circuit 502 and thus, data provided by the latch circuit 502, may be disabled by the appropriate value for the EN2 enable signal. However, Tjandrasuwita does not teach or even suggest that the EN2 enable signal is controlled so that the latch circuit 502 communicates indications of first data to its output terminal in synchronization with a first phase of a clock signal and prevents communication of second data during a second phase of the clock signal. Rather,

Tjandrasuwita teaches use of the EN2 enable signal to prevent the communication of all data, not disabling the latch during a particular phase of a clock signal.

Thus, Tjandrasuwita does not teach or suggest a second circuit that causes a first circuit to communicate indications of first data to an output terminal in synchronization with a first phase of a clock signal and prevent communication of the second data during a second phase of the clock signal. The alleged AAPA does not teach or suggest the missing claim limitations. Therefore, for at least the reason that neither applied reference teaches the second circuit of independent claim 1, a *prima facie* case of obviousness has not been established for claim 1.

Rather than citing specific language from Tjandrasuwita to show where Tjandrasuwita teaches or suggests the missing claim limitations, the Examiner states, "Tjandrasuwita teaches the limitation prevents communication of second data during a second phase of the clock signal (See Final Action, page 3, lines 16-19) with a proper motivation." Advisory Action, 1. Thus, the Examiner acknowledges that Tjandrasuwita does not teach transmitting data during one phase of a clock signal and not transmitting data during a second phase of a clock signal; and sets forth the untenable position that the missing claim limitations would have been obvious to one of ordinary skill in the art.

To establish a *prima facie* case of obviousness, there must be a suggestion or motivation to modify a reference to derive the missing claim limitations. M.P.E.P. § 2143. Furthermore, the Examiner must point to specific language in the prior art establishing the alleged suggestion or motivation to modify a reference to derive the

missing claim limitations. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

Not only does the Examiner fail to show the missing claim limitations and fail to show support for the alleged suggestion or motivation to modify Tjandrasuwita and/or the alleged AAPA to derive the missing claim limitations, the Examiner relies on the general level of skill in the art. The Examiner concludes, "therefore, there is some teaching, suggestion or motivation to do so in the knowledge generally available to one of ordinary skill in the art." Advisory Action, 3. However, the Examiner provides no support for this alleged knowledge in the art and has failed to show any support for this alleged suggestion or motivation, despite previous requests by the Applicant. This is improper, as "rarely, however, will the skill in the art component operate to supply missing knowledge or prior art to reach an obviousness judgment." *Al-Site Corp. v. VSI Int'l, Inc.,* 50 USPQ2d 1161, 1171 (Fed. Cir. 1999). Therefore, for at least the additional, independent reason that the Examiner fails to provide any support for the alleged suggestion or motivation to modify Tjandrasuwita and/or the alleged AAPA to derive the missing claim limitations, a *prima facie* case of obviousness has not been established for claim 1. Claims 2-9 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 1-9 are improper and should be reversed.

B. Can claims 10-14 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 10?

The computer system of independent claim 10 includes a system memory and a processor. The processor includes a wire, a first circuit and a second circuit. The first circuit receives indications of first data that is associated with a first data set and a second data that is associated with a second data set. The second circuit is coupled to the first circuit to cause the first circuit to in a first mode, communicate indications of the first data to the wire and synchronization with a first phase of a clock signal and communicate indications of the second data to the wire in synchronization with a second phase of the clock signal. The second circuit causes the first circuit to in a second mode, communicate indications of the first data to the wire in synchronization with the first phase and prevent communication of the second data during the second phase.

The Examiner rejects independent claim 10 under 35 U.S.C. § 103(a) as being unpatentable in view of the combination of Tjandrasuwita and the AAPA. However, neither the alleged AAPA nor Tjandrasuwita teaches or suggests a second circuit to cause a first circuit to communicate indications of first data to a wire in synchronization with a first phase of a clock signal and prevent communication of the second data during a second phase of the clock signal.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 10 for at least two reasons. First, none of the cited references teaches or suggests all of the claim limitations, as noted above. Secondly, the Examiner relies on the alleged

general level of skill in the art without providing any support for the suggestion or motivation to modify Tjandrasuwita or the alleged admitted prior art so that data communication occurs on a first clock phase and does not occur on a second clock phase. Therefore, for at least these reasons, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 10.

Claims 11-14 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 10-14 are improper and should be reversed.

C. Can claims 15-19 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 15?

The system of independent claim 15 includes double pumped bus circuits that are serially coupled together to form a chain to communicate data from at least two different sets of data. At least one of these bus circuits is capable of being disabled to prevent bits from at least one of the sets of data from being communicated through this bus circuit.

The Examiner rejects independent claim 15 under 35 U.S.C. § 103(a) as being unpatentable over the alleged AAPA and Tjandrasuwita. It is noted that Tjandrasuwita neither teaches nor suggests disabling a double pumped bus circuit from preventing bits from at least one of sets of data from being communicated through the disabled double pumped bus circuit. Furthermore, such a disclosure is not present in the alleged Applicant's admitted prior art. In this manner, the Background of the present application discloses double pumped bus circuits. However, the Background does not mention

disabling the communication of data through one of these circuits. Additionally, the Examiner fails to provide support for the alleged suggestion or motivation to modify the arrangement disclosed in the Background of the present invention or the alleged AAPA to derive the missing claim limitations, but rather improperly relies on the alleged general level of skill in the art. Thus, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 15.

Claims 16-19 are patentable for at least the reason that these claims depend from an allowable claim.

Therefore, the § 103 rejections of claims 15-19 are improper and should be reversed.

D. Can claim 16 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 16?

Claim 16 depends from independent claim 15. Claim 16 states that alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data from being communicated through the bus circuits that are disabled.

The Examiner rejects claim 16 under 35 U.S.C. § 103(a) in view of the combination of Tjandrasuwita and the alleged AAPA. Although Fig. 2 of the present application depicts double pumped bus circuits, the Background section of the application that refers to this figure neither teaches nor suggests that alternate double pumped bus circuits are disabled. Furthermore, this alternate disabling of double pumped bus circuit is neither taught nor suggested by Tjandrasuwita. Additionally, the Examiner provides

no support for a suggestion or motivation for this alternate disabling of double pumped bus circuits. Instead, the Examiner once again relies on the alleged general level of skill in the art and provides no specific citations to any prior art references in support of the Examiner's position. Therefore, for at least these reasons, a *prima facie* case of obviousness has not been established for claim 16.

Thus, the § 103 rejection of claim 16 is improper and should be reversed.

E. Can claims 20-23 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 20?

The method of claim 20 includes receiving first indications of first data that is associated with a first data set and receiving second indications of second data that is associated with a second data set. The method includes in a first mode, communicating first indications to a double pumped bus in synchronization with a first phase of a clock signal and communicating the second indications to the double pumped bus in synchronization with a second phase of the clock signal. The method recites in a second mode, communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

The Examiner rejects independent claim 20 under 35 U.S.C. § 103(a) in view of Tjandrasuwita and the alleged AAPA. However, neither the Background section of the present application nor Tjandrasuwita teaches or suggests communicating first indications of a first set of data to a double pumped bus in synchronization with a first

phase of a clock signal and preventing communication of second indications of second data associated with the second data set to the double pumped bus during a second phase of the clock signal. Furthermore, the Examiner provides absolutely no support for the alleged suggestion or motivation to modify either of these references to derive the missing claim limitations. Thus, for at least these reasons, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 20.

Claims 21-23 are patentable for at least the reason that these claims depend from an allowable claim.

Therefore, the § 103 rejections of claims 20-23 are improper and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: February 18, 2003

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APPENDIX OF CLAIMS

The claims on appeal are:

1. An apparatus comprising:

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

2. The apparatus of claim 1, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

3. The apparatus of claim 2, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

4. The apparatus of claim 2, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

5. The apparatus of claim 4, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

6. The apparatus of claim 5, wherein the logic does not provide the clock signal to the second latch in the second mode.

7. The apparatus of claim 5, wherein the logic comprises:

an AND gate including a first input terminal to receive a mode select signal, a second input terminal to receive the clock signal and an output terminal coupled to a clock input terminal of the second latch.

8. The apparatus of claim 2, further comprising:

a multiplexer including an output terminal that is coupled to the output terminal of the apparatus, the multiplexer alternatively selecting the first and second latch in response to the first and second phases of the clock signal.

9. The apparatus of claim 1, wherein the apparatus comprises a double pumped bus circuit.

10. A computer system comprising:

a system memory; and

a processor coupled to system memory, the processor including:

a wire;

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to the wire in synchronization with a first phase of a clock signal and communicate indications of the second data to the wire in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the wire in synchronization with the first phase and prevent communication of the second data during the second phase.

11. The computer system of claim 10, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

12. The computer system of claim 11, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

13. The computer system of claim 11, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

14. The computer system of claim 13, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

15. A system comprising:

double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data, at least one of the bus circuits being capable of being disabled to prevent bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

16. The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

17. The system of claim 15, wherein each double pumped circuit latches bits from one of the sets of data in response to first edges of a clock signal and furnishes indications of the bits in response to second edges of the clock signal, the first edges being different from the second edges.

18. The system of claim 17, wherein the first edges comprises positive edges of the clock signal.

19. The system of claim 17, wherein the first edges comprises negative edges of the clock signal.

20. A method comprising:

receiving first indications of first data associated with a first data set;

receiving second indications of second data associated with a second data set;

in a first mode, communicating the first indications to a double pumped bus in synchronization with a first phase of a clock signal and communicating the second indications to the double pumped bus in synchronization with a second phase of the clock signal; and

in a second mode, communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

21. The method of claim 20, wherein the receiving the first indications comprises:

latching the first indications one bit at a time.

22. The method of claim 20, wherein the receiving the second indications comprises:

latching the second indications one bit at a time in response to the first mode.

23. The method of claim 20, wherein the communicating during the first mode comprises:

communicating bits of the first data in response to first predefined edges of the clock signal; and

communicating a bits of the second data in response to other predefined edges of the clock signal, said other predefined edges being different from the first predefined clock edges.